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Assistant Commissioner for Patents  
Washington, D.C. 20231

On July 5, 2001

By:

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Attorney Docket No.: 19705-000100US

PATENT

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Technology Center 2100

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

**Bulent Dervisoglu et al.**

Application No.: 09/275,726

Filed: March 24, 1999

For: ON-CHIP SERVICE PROCESSOR  
FOR TEST AND DEBUG OF  
INTEGRATED CIRCUITS

Examiner: D. Ton

Art Unit: 2133

AMENDMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

In response to the Office Action mailed April 4, 2001, please amend the above-identified application as follows:

IN THE CLAIMS:

Please **amend** claims 1, 10 and 15 as follows:

- 1 1. (Amended twice) An integrated circuit having logic blocks comprising  
2 a control unit for performing test and debug operations of said logic blocks of  
3 said integrated circuit;  
4 a memory associated with said control unit, said memory holding instructions  
5 for said control unit; and  
6 a plurality of probe lines responsive to said control unit for carrying system  
7 operation signals at predetermined probe points of said logic blocks, wherein said probe lines  
8 comprise strings of storage elements providing signal paths between said probe points and said